## ABSTRACT

Integrated Circuits (IC) are evolving in terms functionality and diversity. This in turn increased the number of components being integrated in order to function as a system. Basic Ohm's Law suggests that the more load is being connected to a power source, the more current it consumes which equates into higher power consumption. Adding circuitries should not be a burden in terms of power consumption.

This study showed a successful integration of the Self-Cascode Ultra Low Leakage (SCULL) transistor configuration technique into an existing POR designs, namely the POR based on self-biased current source and POR with Accurate Hysteresis, which significantly reduced the power consumption. The design was made possible by combining the Self-Cascode and Ultra Low Leakage transistor configuration techniques that are capable of suppressing leakage current in both static and dynamic state of transistors. The use of SCULL transistor was also able to improve the POR delay significantly while carrying the functionality across different process corners.



Keywords: Self-Cascode Ultra Low Leakage, SCULL, Power-on-Reset, Low Power Consumption