ABSTRACT

Polymorphic gates are logic gates that are able to change their functionality in response to a change in a sensitive variable which can be the supply voltage, temperature or an external signal. This paper presents a new self-checking 3-bit odd parity generator using a newly designed polymorphic gate controlled by an external signal using a new design approach. Six stages make up the new design approach: First, the desired target response of the parity generator is defined. Second, the Boolean equation for the parity generator is derived in order to know the function of the polymorphic gates. Third, the design and construction of the polymorphic gates takes place, which is broken into three sub-stages: the formulation of the truth table of the polymorphic gates, the design and circuit verification and the response evaluation. The fourth stage is the design and construction of the self-checking circuit. The fifth stage is the verification and spice simulation of the candidate circuit using LT Spice ver 4.00n. The last stage is the response evaluation of the self-checking parity generator. The self-checking parity generator circuit consists of two polymorphic NAND/NOR, one polymorphic NAND/OR, one XNOR gate, one XOR gate and one inverter. The parity checker is able to detect the stack-at-fault at any gate without any additional logic and diagnostics signals within the circuit. A fault is indicated by oscillations at the output. The self-checking circuit is fast and guarantees proper operation at any sequence of input combinations without delay. It guarantees appropriate operation at different various frequencies and proper operation at values within ± 50% of the supply voltage. It ensures of low power consumption. Based on the results of the tests done, the self-checking circuit has great potential to be tested on silicon if ever fabrication is to be considered.

Keywords: polymorphic logic gate, self-checking circuit, output logic levels, parity generator, stuck-at-fault