DEVELOPMENT OF CLOCK SYNCRONIZATION FOR DE LA SALLE UNIVERSITY DASMARIÑAS THROUGH INTERNET TIME SERVICE

A Project Study Presented to the Faculty of College of Engineering, Architecture and Technology De La Salle University – Dasmariñas

In Partial Fulfilment of the Requirements for the Degree Bachelor of Science Major in Electronics and Communication Engineering

> CARADA, Peter Paul D. DELA PAZ, Dalton C. DENUYO, Junzen U. LEGASPI, Roland Joseph G.

> > October 2009

Abstract

An abstract of the thesis of Peter Paul Carada, Dalton Dela Paz, Junzen Denuyo and Roland Joseph Legaspi for the Bachelor of Science in Electronics and Communication Engineering presented October 14, 2009.

Title: Development of Clock Synchronization for De La Salle University Dasmariñas using Internet Time Service

Time has been an important variable for humans in their everyday lives. Humans developed things called clocks in order to determine the current time, from sundials to digital clocks; various developments were done in order to predict time accurately. Accuracy in time is very important in our world today. Some analog clocks in De La Salle University do not display time accurately and some does not even function anymore.

The purpose of the present study is to solve the problem of inconsistent time from different clocks in the university by developing a system that will synchronize a clock with the NTP server through the internet. Three digital clocks were built wherein one clock functions as a master and other two as slave clocks. It synchronizes with an NTP server using Network Time Protocol, uses static IP address assigned by the Information Technology Center. The clocks' displays were built using four 4-inch 7-segments that displays the time in 24-hour format.

On the initial test using the DLSU-D network, a problem was encountered. To solve this problem, all the three clocks were converted to stand-alone clocks. The system was then subjected to two sets of tests. The first test measures the discrepancy between a reference clock and the three digital clocks for 8 hours using a 1 megabit per second internet connection. A similar test was done on a 384kbps connection now with the duration of 3 hours to compare the effect of the internet speed on the discrepancy between the reference clock and the 3 devices. The second set of test was the measurement of the time it takes for the clocks to synchronize with the NTP server and like the first test, two different internet connection speed was used.

The data from the first set of test showed an average of below 1 second offset on both connections. On the 1Mbps connection, the average was below 0.3 seconds while the average for the 384kbps connection was below 0.7 seconds. On the second test, the average times measured was approximately 21 seconds. The third test shows that for every 4 hours, the clock which offset is increased 1 second.

iii

TABLE OF CONTENTS

Approval Sheet	i
Abstract	ii
Acknowledgement	iii
Table of Contents	iv
List of Figures	viii
List of Tables	ix
List of Graphs	ix

CHAPTER I-THE PROBLEM AND ITS BACKGROUND

Introduction	1
Background of the Study	2
Statement of the Problem	3
Significance of the Study	4
Scope and Delimitation	4
Conceptual Framework	5
Definition of Terms	7
CHAPTER II-Review of Related Literature and Related Study	
Foreign Literature	8
Foreign Study	11
Local Study	12
Relevance to the Present Study	13

CHAPTER III-METHODS AND PROCEDURES

Research Design	14

Research Methodology and Procedures	14	4
-------------------------------------	----	---

CHAPTER IV-DATA AND RESULTS

CHAPTER V-SUMMARY OF FINDINGS, CONCLUSION RECOMMENDATIONS	I AND
Costing	77
LED Display Driver Source Code	67
LED Display Driver Program Flowchart	64
Main Program Source Code	50
Data and Results Main Controller Program Flowchart	38 48
Project Evaluation	37
E. Integrated Development Environment	34
D. Seven segment Display	30
C. Seven segment LED Driver	26
B. Ethernet Controller	23
A. Main Controller Board	19
Project Structure	19
Project Description	18

Summary of Findings

Conclusion		79
Recommendations	;	79
REFERENCES		81
APPENDICES		
Appendix A-Data S	Sheet	82
Appendix B-Source	e Code Zilog Z8F6421	124
Appendix C-PIC16	F877 Source Code	200
Appendix D-Block Schematic Diagrar	Diagram and Complete n	211
Appendix E-Certific Appendix F-Curric	cation ulum Vitae	212 214

List of Figures

Figure 1.1: Research Paradigm	6
Figure 3.1: Process Overview	15
Figure 4.1: Zilog Z8f6421 Block Diagram	20
Figure 4.2: Pin Configuration of LM7805	21
Figure 4.3: LM317 (Front View)	22
Figure 4.4: Schematic Diagram of Main Controller Circuit	22
Figure 4.5: PCB Layout of the Main Controller Circuit	23
Figure 4.6: Schematic Diagram of the Ethernet Controller Circuit	23
Figure 4.7: Actual Picture of the Ethernet Controller Circuit	25
Figure 4.8: Block Diagram of ENC28J60	26
Figure 4.9: RJ-45 with Internal Magnetics	27
Figure 4.10: Pin Configuration of PIC16F877A	28
Figure 4.11: Schematic Diagram of LED Driver	29
Figure 4.12: PCB with Components Overlay of LED Driver	29
Figure 4.13: Actual Picture of LED Driver	30
Figure 4.14: Schematic Diagram of each Darlington Pair	31
Figure 4.15: Schematic Diagram of 7 Segment LED Display	31
Figure 4.16: Pin Configuration of 7 Segment LED	32
Figure 4.17: PCB Layout for ULN Driver	33
Figure 4.18: Schematic of ULN Driver	35
Figure 4.19: Zilog ZDS II Integrated Development Environment	36
Figure 4.20: MPLAB Integrated Development Environment	41
Figure 4.21: Zilog Program Flowchart	49
Figure 4.22: Operation for SPI	59
Figure 4.23: PIC16F877A Program Flowchart	66
Figure 4.24: Option Register of PIC16F877A	41

List of Tables

Table 4.1: Offset between Desktop Clock and	
Device Using Same NTP Server	38
Table 4.2: Offset using 1Mbps connection	42
Table 4.3: Offset using 384kbps Connection	43
Table 4.4: Connectivity Test Results Using 1Mbps Connection	44
Table 4.5: Connectivity Test Results Using 384Kbps Connection	44
Table 4.6: Accuracy of Clocks without Internet Connection	45
Table 4.7: Reconfigured Clock Accuracy Without Internet Connection	47
Table 4.8: Project Cost Summary	77

List of Graphs

Graph 4.1: Discrepancy of Device 1	39
Graph 4.2: Discrepancy of Device 2	40
Graph 4.3: Discrepancy of Device 3	41